

ABSTRACT

Integrated circuits such as semiconductor memories, image sensors, PLA's, and the like have been formed on rigid, planar substrates such as silicon substrates. This has resulted in shapes without flexibility and limited applicabilities. Further, since multiple circuit elements are continuously formed on a flat surface, it has been impossible to produce a non-defective semiconductor memory unless all the circuit elements are fabricated without defects, making it difficult to improve a yield. It is thus devised to weave or braid linear devices into a fabric shape to prepare a planar semiconductor memory, or to bundle up linear devices to prepare a linear semiconductor memory. The integrated circuit comprising the linear devices is flexible and light-weighted, and is thus usable in various applications. It becomes possible to prepare an integrated circuit by once fabricating linear devices and selecting only non-defective ones therefrom, thereby enabling an improved production yield of integrated circuits.